REMARKS

Claims 1-44 are pending in the present application. Claims 5, 6, 12-14, 16, 20, and 22-24 have been withdrawn in response to a restriction requirement. Claims 7, 8, 21, 25, 30, 34, 35, 39, 40, 41, 42, and 44 have been amended to correct typographic errors and/or to clarify the subject matter recited therein. No new matter is added by the amendments, which find support throughout the specification and figures.

Applicants note with appreciation that the Examiner has allowed claims 9 and 10 and determined that claims 15, 17, and 21 are directed to allowable subject matter. Applicants hereby acknowledge the Examiner's reasons for indication of allowable subject matter. Applicants respectfully note that there may be additional reasons for allowing these claims that have not been specifically cited in addition to or instead of the cited reasons.

The Office Action objects to the title of the invention as not descriptive, and therefore the title is amended to "Memory Module and Memory System Having an Expandable Signal Transmission, Increased Signal Transmission and/or High Capacity Memory ".

The specification has been amended to respond to the objections raised by the Examiner, and therefore it is respectfully requested that the objections be withdrawn.

Claims 7, 8, and 25-44 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 7, 8, 21, 25, 30, 34, 35, 39, 40, 41, 42, and 44 have been amended to respond to these rejections. It is respectfully submitted that the amended claims are definite, and it respectfully requested that the rejection of the claims be withdrawn.

Regarding claim 8, the second transfer gate is discussed in the specification, page 27, lines 4-13. In particular, the on-chip terminator of claim 8 is an element in which a center-tapped termination is turned ON/OFF by a transfer gate, and the center tapped termination is formed of

an intermediate node disposed between two resistors A, B which are connected in series across VDDQ and VSSQ. The node is connected to the bus line. A connection between VDDQ and resistor A is effected by a first transfer gate, while a connection between VSSQ and resistor B is effected by a second transfer gate. It is respectfully submitted that the amended claims are definite, and it respectfully requested that the rejection of the claims be withdrawn.

Regarding claim 37, Applicants respectfully submit that "the level conversion circuit" of lines 17-18 has antecedent basis on line 15. Further regarding claim 37, Applicants respectfully submit that "said open drain type driver" of line 22 has antecedent basis on line 13. It is respectfully submitted that claim 37 is definite, and it respectfully requested that the rejection of the claim be withdrawn.

Claims 1-4, 11, 18, and 19 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,661,690 to Moriarty et al. (hereinafter Moriarty). Applicants respectfully traverse.

Claim 1 relates to a memory module comprising a plurality of memory devices, which share a bus line, on a board. In claim 1, the bus line connects terminals of the plurality of memory devices in a stubless configuration and an end of the bus line is terminated.

Applicants respectfully submit that Moriarty does not disclose, or even suggest, the feature of memory devices connected to a bus line in a stubless configuration. Moriarty apparently discloses a circuit arrangement in which the wiring runs along the long side of the memory module (i.e., in parallel with the connector), and the terminals are disposed on one side or both sides of the module. The input terminals and output terminals are concentrated on one of the right or left side of the module, thus resulting in a small allowable number of wirings. In other words, the allowable number of wiring are limited.

In contrast to Moriarty, the present invention provides a wiring arrangement that runs along (in parallel with) the short side of the module (i.e., at right angles with the connector), and the terminals are disposed on both (upper and rear) surfaces of the module. By this arrangement, the input terminals and the output terminals of the wirings can be disposed broadly over the entire right and left sides, thereby enabling disposition of a far larger number of wirings. Therefore, it is apparent that Moriarty does not disclose or suggest, memory devices connected to a bus line in a stubless configuration, and therefore Moriarty does not anticipate claim 1.

Claims 2-4, 11, 18, and 19 depend from claim 1 and therefore these claims are allowable for at least the same reasons as claim 1 is allowable.

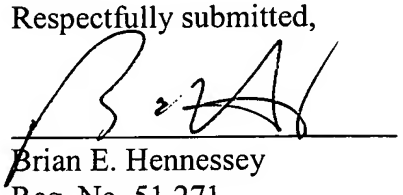
CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that the claims are in condition for allowance. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



Brian E. Hennessey
Reg. No. 51,271

CUSTOMER NO.: 026304

Phone No.: (212) 940-6311
Fax No.: (212) 940-8986/7
ATTORNEY DOCKET NO.: NEKO 20.511
BEH:pm